REMARKS

Claims 1-18 are pending in the current application. Claims 1, 8 and 18 are independent claims. No new matter is added. In view of the below remarks, reconsideration and withdrawal of the rejections is kindly requested.

35 U.S.C. § 103 (A) REJECTION – BROOKS

Claims 1-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Brooks et al. (hereinafter 'Brooks'), U.S. Patent No. 5,786,276. Applicants respectfully traverse this rejection.

The Examiner asserts that "Brooks discloses [Re claim 1] a method of ...etching the silicon nitride film using a plasma generated from an etching gas including CH_2F_2, while maintaining the semiconductor substrate at the process temperature..." Action, p. 2. Furthermore, "But it fails to disclose the exact claimed range. However, in the case where the claimed ranges 'overlap or lie inside ranges disclosed by the prior art' a *prima facie* case of obviousness exists (See MPEP 2144.05)." Action, p. 3.

The Applicant submits with regard to overlapping ranges, the MPEP states:

> "[A] prior art reference that discloses a range encompassing a somewhat narrower claimed range is sufficient to establish a prima facie case of obviousness." *In re Peterson*, 315 F.3d 1325, 1330, 65 USPQ2d 1379, 1382-83 (Fed. Cir. 2003). ***However***, if the reference's disclosed range is ***so broad*** as to encompass a very large number of possible distinct compositions, this might present a situation ***analogous to the obviousness of a species*** when the prior art broadly discloses a genus. *Id.* See also *In re Baird,* 16 F.3d 380, 29 USPQ2d 1550 (Fed. Cir. 1994); *In re Jones,* 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992); MPEP §2144.08.
>
> MPEP §2144.05 (emphasis added)

Applicant submits that Brooks's range, particularly "a wafer backside temperature in the range of approximately 20°C to 100°C" is so broad as to present a situation analogous to the obviousness of a species. See Brooks, col. 4, lines 33-34.

In Section 2144.08, the MPEP states, in determining whether the claimed species or subgenus would have been obvious to one of ordinary skill in the art, "[t]he fact that a claimed species or subgenus is encompassed by a prior art genus is not sufficient by itself to establish a *prima facie* case of obviousness. *In re Baird,* 16 F.3d 380, 382, 29 USPQ2d 1550, 1552 (Fed. Cir. 1994)." MPEP §2144.08. Therefore, the fact that Brooks claims a specific surface range of approximately 20°C to 100°C, by itself, is not sufficient to establish a *prima facie* case of obviousness.

Applicant submits that "[a] proper obviousness analysis involves a three-step process. First, Office personnel should establish a *prima facie* case of unpatentability considering the factors set out by the Supreme Court in *Graham v. John Deere.* See, e.g., *In re Bell,* 991 F.2d 781, 783, 26 USPQ2d 1529, 1531 (Fed. Cir. 1993) ('The PTO bears the burden of establishing a case of *prima facie* obviousness.')." MPEP §2144.08. Specifically,

> *Graham v. John Deere Co.,* 383 U.S. 1, 17-18 (1966), requires that to make out a case of obviousness, one must:
>
> (A) determine the scope and contents of the prior art;
>
> (B) ***ascertain the differences between the prior art and the claims in issue***;
>
> (C) determine the level of skill in the pertinent art; and
>
> (D) evaluate any evidence of secondary considerations.
>
> MPEP §2144.08 (emphasis added)

Thus, the Examiner should consider the results of the temperature range of the claimed application as it differs from the temperature range taught in Brooks. In doing so,

> In *Stratoflex, Inc. v. Aeroqup Corp.,* 713 F.2d 1530, 1537, 218 USPQ 871, 877 (Fed. Cir. 1983), the Court noted that 'the question under 35 U.S.C. § 103 is not whether the differences [between the claimed invention and the prior art] would have been obvious' but 'whether the claimed invention *as a whole* would have been obvious.' (emphasis in original).
>
> MPEP §2144.08

Accordingly, Applicant submits in order for the Examiner to establish a *prima facie* case of obviousness between the difference in the claimed invention and Brooks, he must answer the question: Would the claimed invention ***as a whole*** have been obvious to one of ordinary skill in the art in view of Brooks? In view of the arguments given below, Applicant submits the claims as a whole would not have been obvious.

Applicants submit that Brooks discloses a method of *chemical downstream etching (CDE)* wherein a plasma composed of CH_3F gas and/or gas CH_2F_2 in combination with CF_4 and oxygen to etch a wafer or other like workpiece which has exposed silicon nitride adjacent to exposed silicon oxide and/or exposed silicon. Brooks teaches "[t]he backside temperature of wafer 120 is more preferably maintained at approximately 30°C or less." Brooks, col. 4, lines 34-36. Moreover, Tables 1A-1C disclose a chuck temperature of 30°C $\pm$ 5 wherein "the recipe ranges of Table 1A have been found to be particularly advantageous" and the "recipes of Tables 1B and 1C have been found to be useful." Brooks, col. 3, lines 4-6 and 25-26.

However, claim 1 of the present invention recites a method of etching a silicon nitride film comprising "heating the semiconductor substrate to a process temperature of at least about 40°C"; see, for example, the specification, p. 9, paragraph [0029].

Moreover, the exemplary embodiments of the present invention teach that the temperature difference may overcome the low etch rate deficiencies of prior art U.S. Patent Application No. 2002-84254 and Japanese Laid Open Patent Publication No. 2001-203208, and likewise Brooks, because "[these methods] of etching the silicon nitride film, despite improving the selectivity, [have] a relatively low etch rate because the silicon nitride film is etched at a temperature of below about 30°C," wherein "[a]ccording to the present invention, because the silicon nitride film formed on a semiconductor substrate is etched using an etching gas including CH_2F_2 at a temperature of above about 40°C, the etching rate of the silicon nitride film may be increased relative to the etching rate of a silicon oxide film.

Namely, the silicon nitride film may be etched five times more rapidly than the silicon oxide film." Specification, p. 5, paragraph [0013] and p. 12, paragraph [0036].

Therefore, Applicants submit that Brooks fails to disclose the relationship between the etch rate of the silicon nitride and silicon oxide films in relation to the temperature of the substrate as taught by the example embodiments of the present application. Specifically, the silicon nitride film may be etched at a rate of five times more than the etch rate of the silicon oxide film wherein, at least, the process temperature is above about 40°C.

In view of the foregoing argument and to expedite prosecution of the present application, Applicants submit that claims 1, 8 and 13 have been amended to include the feature "wherein the etching gas has an etching selectivity of above about five between the silicon nitride film and the buffer layer at the process temperature" or a similar recitation. This feature is added to help distinguish the claims of the present invention from the prior art.

Accordingly, Brooks fails to teach "wherein the etching gas has an etching selectivity of above about five between the silicon nitride film and the buffer layer at the process temperature" as recited in claim 1 of the present invention.

As such, Applicants respectfully request that the Examiner reconsider and withdraw the rejection of claim 1.

Reconsideration and withdrawal of the rejection to claims 2-7, by virtue of at least their dependency on claim 1, is kindly requested.

35 U.S.C. § 103(a) - ZHU

Claims 1-7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zhu et al. (hereinafter 'Zhu'), U.S. Patent Publication No. 2002/0182880. In view of the following remarks, Applicants respectfully traverse this rejection.

The Examiner asserts,

> Zhu discloses [Re claim 1] a method of etching a silicon nitride film comprising...heating the semiconductor substrate to a process temperature in the range of 0-100C and etching the silicon nitride film using a plasma generated from an etching gas including CH_2F_2, while maintaining the semiconductor substrate at the process temperature...[Re claim 6] wherein in the process temperature is between about 60 and about 100C; (See Table 2, pars. 42-46 and 49)...But it fails to disclose the exact claimed range.
>
> Action, p. 3.

Applicants agree that Zhu fails to disclose an exact range, but do not agree with the Examiner's reasoning.

Further to the arguments given above, Applicants submit that Zhu is silent with regards to a temperature range for the semiconductor substrate. Contrary to the Examiner's assertion, as shown below, paragraph [0046] of Brooks discusses controlling the temperature of the *substrate support*, as such,

> The ***substrate support*** supporting the semiconductor substrate undergoing etching preferably cools the substrate enough to prevent burning of any photoresist on the substrate, e.g., maintain the substrate below 140°C. In high and medium density plasma reactors, it is sufficient to cool the ***substrate support*** to a temperature of -20 to 40°C. The ***substrate support*** can include a bottom electrode for supplying an RF bias to the substrate during processing thereof and an ESC for clamping the substrate. For example, the substrate can comprise a silicon wafer which is electrostatically clamped and cooled by supplying helium at a desired pressure between the wafer and top surface of the ESC. In order to maintain the wafer at a desired temperature of, for example, 0 to 100°C., the He can be maintained at a pressure of 2 to 30 Torr in the space between the wafer and the
>
> Action, p. 4.

Zhu merely mentions the temperature range of 0 to 100°C as an example of a range that can be reached if the helium is maintained at a pressure of 2 to 30 Torr. It is does not teach a desired temperature range for performing the outlined method.

As for Tables 1 and 2 and paragraphs [0048] and [0049], there is no mention of a semiconductor substrate or process temperature for the claimed method, only a "...20 to 40°C ***bottom electrode*** temperature..." Zhu, p. 4, paragraph [0048] and p. 5, paragraph [0049].

Thus, Zhu fails to disclose the relationship, discussed above, as taught by an example embodiment of the present invention.

As such, Zhu fails to disclose "wherein the etching gas has an etching selectivity of above about five between the silicon nitride film and the buffer layer at the process temperature" as recited in independent claim 1.

Moreover, the Examiner asserts "where the claimed ranges 'overlap or lie inside ranges disclosed by the prior art' a *prima facie* case of obviousness exists (See MPEP 2144.05)." Action, p. 4. However, the Applicants maintain that since Zhu is silent about a semiconductor substrate temperature range, no *prima facie* case of obviousness has been established.

Accordingly, Applicants respectfully request that the Examiner reconsider and withdraw the rejection of independent claim 1.

Reconsideration and withdrawal of the rejection to claims 2-7, by virtue of at least their dependency on independent claim 1, is kindly requested.

35 U.S.C. § 103(a) – BUYNOSKI, BROOKS AND ZHU

Claims 8-12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Buynoski et al. (hereinafter 'Buynoski), U.S. Patent No. 6,300,203 in view of Brooks and Zhu. Applicants respectfully traverse this rejection.

The Examiner asserts,

> Referring to Figs. 8-12 and related text, Buynoski discloses a method of manufacturing a semiconductor device comprising: forming a gate insulation film 106 on a semiconductor substrate 102; forming a gate structure having a gate electrode 108 and a gate mask 110 on the gate insulation film, forming a first buffer layer 112 including silicon oxide on the gate structure and inherently on the semiconductor substrate; forming a silicon nitride film on the first buffer layer to form a gate spacer along a sidewall of the gate structure.
>
> Action, p. 4.

Applicants submit that the Examiner has improperly interpreted Buynoski. Figures 8-12 of Buynoski are directed to prior art reference "...U.S. Patent 5,960,270 for forming an in-laid gate electrode for use in MOS and CMOS devices..." Buynoski, col. 4, lines 63-64. Furthermore, Buynoski distinguishes itself over patent '270, among other references, as follows,

> However, all of the methods conventionally employed (or proposed) for forming such ***high–k dielectric layers*** utilize chemical vapor deposition ("CVD") or physical vapor deposition ("PVD") processes which incur a number of disadvantages and drawbacks, including: (1) energetic ion bombardment accompanying PVD-type processing resulting in degradation of the oxide/Si interface; (2) presence of free oxygen during PVD- and/or CVD-type processing resulting in ***unwanted reaction*** with Si substrate material to form ***low-k SiO_2-based dielectric materials***; and (3) entrapment of ion bombardment species during PVD-type processing, along with associated radiation damage of the deposited high-k dielectric films.
>
> Buynoski, col. 6, lines 38-50 (emphasis added).

As such, Buynoski is directed to a method of manufacturing a semiconductor device wherein a *high dielectric layer* forms a gate insulation layer that prevents or reduces oxygen access to the substrate surface so as to inhibit the formation of a *low-k* layer. Specifically,

> [T]he electroplated precursor layer is controllably reacted with oxygen or with oxygen and the semiconductor substrate material to form a suitably thick gate insulation layer, preferably a ***high-k*** refractory or lanthanum series transition metal oxide or metal silicate layer, reaction of the precursor layer being carefully controlled so as to terminate prior to onset of reaction of the underlying substrate with oxygen to form an ***unwanted low-k layer***, e.g. of SiO_2.
>
> Buynoski, col. 10, lines 27-34 (emphasis added).

The gate insulation layer of Buynoski includes "...Zr, Hf, La, Lu, Eu, Pr, Nd, Gd, Dy, and alloys and mixtures thereof..." Buynoski, col. 10, lines 43-44.

Furthermore, Buynoski teaches,

> [T]he metal precursor layer with oxygen and the semiconductor substrate material is preferably accomplished by thermal oxidation in an oxygen-containing atmosphere, for example, at about 400-500°C. for about 10-20 min. However, given the present disclosure and objectives of the invention, suitable electrolytic or thermal oxidation conditions for reaction of the

> precursor layer for use in a given application can be readily determined by one of ordinary skill in the art.
>
> Buynoski, col. 11, lines 40-48.

Thus, Buynoski does not disclose a specific process temperature.

Contrary, an example embodiment of the present invention is directed to a method of manufacturing a semiconductor device wherein the gate insulation layer 16 may be comprised of silicon oxide (SiO), a *low-k dielectric* material, which in turn may form a *low-k* dielectric first buffer layer 22. Moreover, the process temperature is of at least about 40°C and preferably between 60 to 100°C.

Thus, Buynoski also fails to disclose the relationship, discussed above, as taught by an example embodiment of the present invention.

Brooks or Zhu fail to render claim 8, for reasons similar to claim 1, obvious to one skilled in the art. Buynoski in view of Brooks or Zhu fails to disclose or teach "wherein the etching gas has an etching selectivity of above about five between the silicon nitride film and the buffer layer at the process temperature" as recited in claim 8. Therefore, claims 9-12, by virtue of at least their dependency on claim 8, are also patentable over Buynoski in view of Brooks or Zhu.

Reconsideration and withdrawal of this rejection is requested.

35 U.S.C. § 103(a) – BUYNOSKI, BROOKS, ZHU AND TSENG

Claims 13-18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Buynoski in view of Brooks or Zhu and further in view of Tseng, U.S. Patent 5,733,808. Applicants respectfully traverse this rejection in view of the following remarks.

The Examiner asserts that "...the missing limitations are well known in the art because Tseng discloses the forming of a second buffer layer 16 and a contact hole through the second buffer and the etch stop layer 18..." Action, p. 5.

Buynoski in view of Brooks and Zhu fails to render claim 8 obvious to one skilled in the art, as discussed above. Tseng discloses a method of manufacturing a cylindrical capacitor for a DRAM; and accordingly teaches "a dry oxidation (e.g., dry O_2) at a temperature in the range of between about 700° and 900°C." Tseng, col. 6, lines 29-31.

For analogous reasons as given above with regard to claim 8 over Buynoski in view of Brooks or Zhu, Tseng also fails to disclose "wherein the etching gas has an etching selectivity of above about five between the silicon nitride film and the buffer layer at the process temperature" as recited in claim 8.

Claims 13-17, by virtue of at least their dependency on claim 8, are also patentable over Buynoski in view of Brooks or Zhu and further in view of Tseng.

Reconsideration and withdrawal of this rejection is requested.

With regard to claim 18, Applicants submit that in view of the arguments given above with regard to claims 1, 8, and 13-17 over Buynoski in view of Brooks or Zhu and further in view of Tseng, claim 18 is allowable by at least its dependency on claim 1.

Applicants respectfully request that the Examiner reconsider and withdraw the rejection of claim 18.

CONCLUSION

Accordingly, in view of the above amendments and remarks, reconsideration of the objections and rejections and allowance of each of claims 1-18 in connection with the present application is earnestly solicited.

Should there be any outstanding matters that need to be resolved in the present application, the Examiner is respectfully requested to contact the undersigned at the telephone number below.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 08-0750 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

HARNESS, DICKEY, & PIERCE, P.L.C.

By _____
John A. Castellano, Reg. No. 35,094

P.O. Box 8910
Reston, Virginia 20195
(703) 668-8000

JAC/CDW